Notice of Allowability	Application No.	Applicant(s)	
	09/468,051	HARTNETT ET AL.	
	Examiner	Art Unit	
	William H. Wood	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *14 February 2005*.

2. ☒ The allowed claim(s) is/are *1-7 and 21-46*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☒ to Paper No./Mail Date *6/25/02*.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *071805* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Beth McMahon on 19 July 2005.

The application has been amended as follows:

Claim 1

For use in an instruction processor that executes instructions included in a predetermined instruction set at an execution rate determined by a system clock signal, a synchronous instruction pipeline, comprising:

a pipeline execution circuit to process a first predetermined number of instructions simultaneously, each of said first predetermined number of instructions being in a respectively different stage of execution within said pipeline execution circuit, instructions being capable of advancing to a next stage of execution within said pipeline execution circuit at a time determined by the system clock signal; and

a pipeline fetch circuit coupled to provide each of the first predetermined number of instructions directly from one stage of said pipeline fetch circuit to one stage of said pipeline execution circuit, the pipeline fetch circuit to retain a second predetermined

number of instructions simultaneously, each of said second predetermined number of instructions being in a respectively different stage of processing within said pipeline fetch circuit, an instruction being capable of advancing to a next stage of execution within said pipeline fetch circuit at a time determined by the system clock signal and independently of the times at which instructions advance to a next stage of execution within said pipeline execution circuit.

Claim 21

For use in an instruction processor, a synchronous pipeline circuit, comprising:

an execution circuit to provide a first predetermined number of execution stages, each being capable of performing a respective processing operation on a respective instruction; wherein an instruction is capable of advancing to a next stage of processing within the execution circuit at a time determined by a system clock signal; and

a fetch circuit coupled to the execution circuit to provide a second predetermined number of fetch stages, each fetch stage being capable of performing a respective pre-execution operation on a respective instruction, wherein an instruction is capable of advancing to a next stage of processing within the fetch circuit at a time determined by the system clock signal, the fetch circuit to transfer each instruction processed by the fetch circuit directly from one of the fetch stages to one of the execution stages;[,]

wherein ones of the instructions processed within the fetch stages being capable of advancing to different available fetch stages independently of whether instructions are advancing within the execution stages.

Claim 27

A synchronous pipeline circuit for processing instructions within a data processing system, comprising:

a first predetermined number of fetch stages to simultaneously process at least a first predetermined number of instructions, wherein an instruction is capable of advancing to a next stage of processing within the fetch stages at a time determined by a system clock signal;

a second predetermined number of execution stages to simultaneously process a second predetermined number of instructions, wherein an instruction is capable of advancing to a next stage of processing within the execution stages at a time determined by the system clock signal, each instruction being received directly from one of the fetch stages by one of the execution stages; and

wherein at least one of the fetch stages is capable of providing an instruction to a different one of the fetch stages that is ready to receive an instruction irrespective of movement of instructions between the execution stages.

Claim 32

A synchronous instruction pipeline to execute instructions, comprising:

an execution circuit having a first predetermined number of execution stages to execute a first predetermined number of instructions ~~substantially~~ simultaneously,

wherein an instruction is capable of advancing to a next stage of processing within the execution circuit at a time determined by a system clock signal; and

a fetch circuit having a second predetermined number of fetch stages to perform pre-execution operations on at least a second predetermined number of instructions ~~substantially~~ simultaneously, wherein an instruction is capable of advancing to a next stage of processing within the fetch circuit at a time determined by the system clock signal, one of the fetch stages being coupled to provide each instruction processed by the fetch circuit directly to one of the execution stages, and at least one of the at least second predetermined number of instructions being capable of advancing between different ones of the fetch stages regardless of whether an instruction is being transferred by the fetch circuit to the execution circuit.

Claim 40

A method of processing instructions within a synchronous pipeline of an instruction processor, comprising:

a.) performing pre-execution operations on a first predetermined number of instructions ~~substantially~~ simultaneously within a ~~first~~ predetermined number of fetch stages in the pipeline, wherein an instruction is capable of advancing to a next stage of processing within the fetch stages at a time determined by a system clock signal;

b.) executing a second predetermined number of instructions ~~substantially~~ simultaneously within a ~~second~~ predetermined number of execution stages of the pipeline, wherein an instruction is capable of advancing to a next stage of processing

within the execution stages at a time determined by the system clock signal, wherein each of the second predetermined number of instructions were received directly from one of the fetch stages by one of the execution stages; and

c.) processing instructions such that ~~allowing~~ one or more of the first predetermined number of instructions ~~to~~ advance between ones of the fetch stages independently of whether any of the second predetermined number of instructions are advancing between ones of the execution stages.

Claim 46

A pipeline circuit for use in an instruction processor, comprising:

instruction fetch means for performing pre-execution operations of a first predetermined number of instructions ~~substantially~~ simultaneously within a ~~first~~ predetermined number of fetch stages, wherein an instruction is capable of advancing to a next stage of pre-execution operation at a time determined by a system clock signal;

instruction execution means for executing a second predetermined number of instructions ~~substantially~~ simultaneously within a ~~second~~ predetermined number of execution stages, wherein an instruction is capable of advancing to a next stage of execution at a time determined by the system clock signal, each of the second predetermined number of instructions being received directly from one of the fetch stages by one of the execution stages; and wherein

the instructions fetch means includes means for allowing at least one of the first predetermined number of instructions to advance within the fetch stages irrespective of whether instructions are advancing within the execution stage.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: the prior art of record fails to teach or suggest the claimed invention. Specifically, the prior art of record fails to teach or suggest fetch stages, wherein an instruction is capable of advancing to a next stage of processing within the fetch stages at a time determined by the system clock signal; execution stages, wherein an instruction is capable of advancing to a next stage of processing within the execution stages at a time determined by the system clock signal, each instruction being received directly from one of the fetch stages by one of the execution stages; and fetch stage is capable of providing an instruction to a different one of the fetch stages irrespective of the movement of instructions between the execution stages, as recited in independent claim 27. Additional independent claims 1, 21, 32, 40 and 46 are allowed for similar reasons.

The prior art of record, **Bhamidipati** et al. (USPN 6,112,295), disclosed a queue system for making sections of execution pipelines independent in operation. However, **Bhamidipati** failed to disclose the independent claims as recited, including instructions passing from one fetch stage directly to one execution stage.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)-272-3736. The examiner can normally be reached 9:00am - 5:30pm Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)-272-3719. The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
July 23, 2005

KAKALI CHAKI
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